Notice of Allowability	Application No.	Applicant(s)	
	09/923,604	HAPKE, FRIEDRICH	
	Examiner	Art Unit	
	John P. Trimmings	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *BPAI action dated 3/27/2006*.

2. ☒ The allowed claim(s) is/are *1-3*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20060710* .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

DETAILED ACTION

1. In view of the action by the Board of Patent Appeals and Interferences dated 3/27/2006, the examiner withdraws all rejections of claims 1-3.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to the applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Michael J. Ure on 7/19/2006.

The claims as recorded in the PTO database (eDAN) for the amendment submitted on 3/14/2004 should start on a separate page. Since the claims as amended on 3/14/2004 are non-compliant, the examiner wishes to clarify the record with a full claim listing. The examiner has therefore rewritten all claims 1-3 as they should appear in the patent publication, as follows:

Claim 1. An arrangement for testing an integrated circuit comprising a combinational logic system, and a test circuit, which arrangement performs a test of the behavior of the combinational logic system in comparison with test software which emulates the nominal behavior of the integrated circuit, the arrangement comprising:

two identical software models of the combinational logic system to be tested, in which a test sample is applied for test purposes to a first of these software models and whose output signals are coupled to a second of these software models;

wherein the test circuit, in a test mode, applies a first test sample in a first test clock cycle to the input of the combinational logic system of the integrated circuit and receives the output signal in a buffer memory, and which feeds back this output signal as a second test sample in a second test clock cycle to the input of the combinational logic system and again receives the output signal of the combinational logic system in the buffer memory

wherein, at the end of the second test clock cycle, the arrangement compares the results of the combinational logic system of the integrated circuit in the buffer memory with the results of the second software model.

Claim 2. The arrangement as claimed in claim 1, characterized in that the buffer memory is constituted as a shift register by means of which the test samples are read and/or written.

Claim 3. A method of testing an integrated circuit comprising a combinational logic system, and a test circuit, in which method the behavior of the combinational logic system is compared with test software which emulates the nominal behavior of the integrated circuit, the method comprising:

providing two identical software models of the combinational logic system to be tested, in which a test sample is applied for test purposes to a first of these software models and whose output signals are coupled to a second of these software models;

wherein the test circuit, in a test mode, applies a first test sample in a first test clock cycle to the input of the combinational logic system of the integrated circuit and receives the output signal in a buffer memory and which feeds back this output signal as a second test sample in a second test clock cycle to the input of the combinational logic system and again receives the output signal of the combinational logic system in the buffer memory

wherein, at the end of the second test clock cycle, the arrangement compares the results of the combinational logic system of the integrated circuit in the buffer memory with the results of the second software model.

Allowable Subject Matter

3. Claims 1-3 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John P Trimmings
Examiner
Art Unit 2138

jpt

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100